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09/892,291	06/25/2001	Joseph Weiyeh Ku	10008039-1	2125

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EXAMINER	
MANOSKEY, JOSEPH D	

ART UNIT	PAPER NUMBER
2113	

DATE MAILED: 08/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/892,291	KU, JOSEPH WEIYEH	
	Examiner	Art Unit	
	Joseph Manoskey	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9 and 12-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,12-24,26-29,31,32 and 34-36* is/are rejected.

7)☒ Claim(s) *25, 30, 33, and 37* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-3, 5, 6, 13, 14, 16, 17, 20, 21, 23, 24, 26-29, 31, 32, and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shephard, III et al., U.S. Patent 5,633,877, hereinafter referred to as "Shephard", in view of Swoboda et al., U.S. Patent 6,704,895, hereinafter referred to as "Swoboda".

3. Referring to claim 1, Shephard discloses a method for chip testing, Shephard describes scanning in instructions to the BIST, (See Col. 1, lines 64-67). Shephard teaches the instructions scanned in being logical test vectors, these test vectors are interpreted to constitute a test algorithm (See Col. 1, lines 60-67). Shephard discloses testing the chip according to the algorithm, gathering the results and scanning them out (See Col. 2, lines 48-53). Shephard does not explicitly teach the BIST being connected to a computer tester via a communications link, however Shephard does teach the system being programmable and instructions being scanned into the system (See Col.

1, lines 50-51 and Col. 2, lines 48-49), this is interpreted as the system being connected to an outside tester via a link.

Swoboda teaches methods that provide improved testability of systems (See Col. 2, line 60 to Col. 3, line 15). Swoboda teaches the system including a host computer attached to the system under test for emulation, which is interpreted as a computer tester communicatively linked to chip for testing (See Fig. 2, and Col. 7, lines 28-43).

It would be obvious to one of ordinary skill in the art at the time of the invention to combine the computer tester and communications link of Swoboda with the programmable BIST of Shephard. This would have been obvious to one of ordinary skill in the art because it allows the programs to be scanned into the target chip (See Swoboda, Col. 8, lines 23-54).

4. Referring to claim 2, Shephard and Swoboda teach all the limitations (See rejection of claim 1) including the method scanning in subsequent test scenarios (See Col. 2, line 53).

5. Referring to claim 3, Shephard and Swoboda disclose all the limitations (See rejection of claim 1) including the testing being of a memory array of the chip (See Col. 1, lines 50-52).

6. Referring to claim 5, Shephard and Swoboda teach all the limitations (See rejection of claim 3) including the results of the test being the failed address (See Col. 3, lines 18-20).

7. Referring to claim 6, Shephard and Swoboda disclose all the limitations (See rejection of claim 5) including the testing writing the data into the array, reading it out of the array, comparing the data read out with the expected data, and providing the address of the failed addresses (See Col. 3, lines 13-20).

8. Referring to claim 13, Shephard discloses a programmable BIST for chip testing, Shephard describes scanning in instructions to the BIST, (See Col. 1, lines 49-50 and 64-67). Shephard teaches the instructions scanned in being logical test vectors, these test vectors are interpreted to constitute a test algorithm (See Col. 1, lines 60-67). Shephard discloses testing the chip according to the algorithm, gathering the results and scanning them out (See Col. 2, lines 48-53). Shephard does not explicitly teach the BIST being connected to a computer tester via a communications link, however Shephard does teach the system being programmable and instructions being scanned into the system (See Col. 1, lines 50-51 and Col. 2, lines 48-49), this is interpreted as the system being connected to an outside tester via a link.

Swoboda teaches methods that provide improved testability of systems (See Col. 2, line 60 to Col. 3, line 15). Swoboda teaches the system including a host computer

attached to the system under test for emulation, which is interpreted as a computer tester communicatively linked to chip for testing (See Fig. 2, and Col. 7, lines 28-43).

It would be obvious to one of ordinary skill in the art at the time of the invention to combine the computer tester and communications link of Swoboda with the programmable BIST of Shephard. This would have been obvious to one of ordinary skill in the art because it allows the programs to be scanned into the target chip (See Swoboda, Col. 8, lines 23-54).

9. Referring to claim 14, Shephard and Swoboda disclose all the limitations (See rejection of claim 13) including the testing being of a memory array of the chip (See Col. 1, lines 50-52).

10. Referring to claim 16, Shephard and Swoboda teach all the limitations (See rejection of claim 14) including the results of the test being the failed address (See Col. 3, lines 18-20).

11. Referring to claim 17, Shephard and Swoboda disclose all the limitations (See rejection of claim 16) including the testing including writing the data into the array, reading it out of the array, comparing the data read out with the expected data, and providing the address of the failed addresses (See Col. 3, lines 13-20).

12. Referring to claim 20, Shephard discloses a system for chip testing, Shephard describes scanning in instructions to the BIST, (See Fig. 2 and 3, and Col. 1, lines 64-67). Shephard teaches the instructions scanned in being logical test vectors, these test vectors are interpreted to constitute a test algorithm (See Col. 1, lines 60-67). Shephard discloses testing the chip according to the algorithm, gathering the results and scanning them out (See Col. 2, lines 48-53). Shephard does not explicitly teach the BIST being connected to a computer tester via a communications link, however Shephard does teach the system being programmable and instructions being scanned into the system (See Col. 1, lines 50-51 and Col. 2, lines 48-49), this is interpreted as the system being connected to an outside tester via a link.

Swoboda teaches methods that provide improved testability of systems (See Col. 2, line 60 to Col. 3, line 15). Swoboda teaches the system including a host computer attached to the system under test for emulation, which is interpreted as a computer tester communicatively linked to chip for testing (See Fig. 2, and Col. 7, lines 28-43).

It would be obvious to one of ordinary skill in the art at the time of the invention to combine the computer tester and communications link of Swoboda with the programmable BIST of Shephard. This would have been obvious to one of ordinary skill in the art because it allows the programs to be scanned into the target chip (See Swoboda, Col. 8, lines 23-54).

13. Referring to claim 21, Shephard discloses a system for chip testing, Shephard describes scanning in instructions to the BIST, (See Fig. 2 and 3, and Col. 1, lines 64-

67). Shephard teaches the instructions scanned in being logical test vectors, these test vectors are interpreted to constitute a test algorithm (See Col. 1, lines 60-67). Shephard discloses the testing being of a memory array of the chip (See Fig. 2 and Col. 1, lines 50-52). Shephard discloses testing the chip according to the algorithm, gathering the results and scanning them out (See Col. 2, lines 48-53). Shephard does not explicitly teach the BIST being connected to a computer tester via a communications link, however Shephard does teach the system being programmable and instructions being scanned into the system (See Col. 1, lines 50-51 and Col. 2, lines 48-49), this is interpreted as the system being connected to an outside tester via a link.

Swoboda teaches methods that provide improved testability of systems (See Col. 2, line 60 to Col. 3, line 15). Swoboda teaches the system including a host computer attached to the system under test for emulation, which is interpreted as a computer tester communicatively linked to chip for testing (See Fig. 2, and Col. 7, lines 28-43).

It would be obvious to one of ordinary skill in the art at the time of the invention to combine the computer tester and communications link of Swoboda with the programmable BIST of Shephard. This would have been obvious to one of ordinary skill in the art because it allows the programs to be scanned into the target chip (See Swoboda, Col. 8, lines 23-54).

14. Referring to claim 23, Shephard and Swoboda teach all the limitations (See rejection of claim 1) including the use of output buffers, this is interpreted as collecting a

set of failure information further comprising temporarily storing the failure information to a buffer on the chip (See Fig. 42 of Swoboda).

15. Referring to claim 24, Shephard and Swoboda disclose all the limitations (See rejection of claim 1) including the chip having a scan test interface, this is interpreted as a communication module on the chip for transmitting failure information (See Fig. 4 of Swoboda).

16. Referring to claim 26, Shephard and Swoboda teach all the limitations (See rejection of claim 1) including the chip and computer exchange messages over a serial bus protocol (See Swoboda, Col. 7, lines 30-33).

17. Referring to claim 27, Shephard and Swoboda disclose all the limitations (See rejection of claim 1) including the tester being a personal computer (See Fig. 2 of Swoboda).

18. Referring to claim 28, Shephard and Swoboda teach all the limitations (See rejection of claim 13) including the use of output buffers, this is interpreted as collecting a set of failure information further comprising temporarily storing the failure information to a buffer on the chip (See Fig. 42 of Swoboda).

19. Referring to claim 29, Shephard and Swoboda disclose all the limitations (See rejection of claim 13) including the chip having a scan test interface, this is interpreted as a communication module on the chip for transmitting failure information (See Fig. 4 of Swoboda).

20. Referring to claim 31, Shephard and Swoboda teach all the limitations (See rejection of claim 20) including the use of output buffers, this is interpreted as collecting a set of failure information further comprising temporarily storing the failure information to a buffer on the chip (See Fig. 42 of Swoboda).

21. Referring to claim 32, Shephard and Swoboda disclose all the limitations (See rejection of claim 20) including the chip having a scan test interface, this is interpreted as a communication module on the chip for transmitting failure information (See Fig. 4 of Swoboda).

22. Referring to claim 34, Shephard and Swoboda disclose all the limitations (See rejection of claim 21) including the tester being a personal computer (See Fig. 2 of Swoboda).

23. Claims 4, 7, 8, 12, 15, 18, 19, 22, 35, and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shephard in view of Swoboda and Bhavsar et al., U.S. Patent 6,408,401, hereinafter referred to as "Bhavsar".

24. Referring to claim 4, Shephard and Swoboda teach all the limitations (See rejection of claim 3) except for the generating a bit-map from the failure information of failed bit locations within the memory array, however Shephard does disclose identifying failed addresses within the memory array (See Col. 3, lines 18-20). Bhavsar teaches testing a memory with a BIST and generating bit-map of the failed memory (See Col. 4, lines 30-32). It would be obvious to one of ordinary skill in the art at the time of the invention to combine the bit-map generating of Bhavsar with the testing method of Shephard and Swoboda. This would have been obvious to one of ordinary skill in the art at the time of the invention to do because it allows for a repair solution to be determined (See Bhavsar, Col. 1, lines 48-49).

25. Referring to claim 7, Shephard and Swoboda disclose all the limitations (See rejection of claim 6) except for adding failed bit locations of the failed address, however Shephard does disclose identifying failed addresses within the memory array (See Col. 3, lines 18-20). Bhavsar teaches testing a memory with a BIST and generating bit-map of the failed memory, it is interpreted that the bit-map contains the failed bits of the failed memory location (See Col. 4, lines 30-32). It would be obvious to one of ordinary skill in the art at the time of the invention to combine the bit-map generating of Bhavsar with the testing method of Shephard and Swoboda. This would have been obvious to one of ordinary skill in the art at the time of the invention to do because it allows for a repair solution to be determined (See Bhavsar, Col. 1, lines 48-49).

26. Referring to claim 8, Shephard and Swoboda disclose all the limitations (See rejection of claim 1) except for repairing the chip using redundancy allocation techniques based on the set of failure information. Bhavsar teaches using spare rows and/or columns to replace failed ones (See Col. 2, lines 22-29). Bhavsar also teaches the repair solution being based on extracted failure information from the test (See Col. 4, lines 64-65). It would be obvious to one of ordinary skill in the art at the time of the invention to combine the repair scheme with redundancy of Bhavsar with the chip testing method of Shephard and Swoboda. This would have been obvious to one of ordinary skill in the art at the time of the invention to do this because the scheme of Bhavsar provides a higher yield of chips during manufacture (See Col. 2, lines 2-5).

27. Referring to claim 12, Shephard discloses a method for chip testing, Shephard describes scanning in instructions to the BIST, (See Col. 1, lines 64-67). Shephard discloses the testing being of a memory array of the chip (See Col. 1, lines 50-52). Shephard teaches the instructions scanned in being logical test vectors, these test vectors are interpreted to constitute a test algorithm (See Col. 1, lines 60-67). Shephard discloses testing the chip according to the algorithm, gathering the results and scanning them out (See Col. 2, lines 48-53). Shephard also discloses the testing including writing the data into the array, reading it out of the array, comparing the data read out with the expected data, and providing the address of the failed addresses (See Col. 3, lines 13-20).

Shephard does not teach the generating a bit-map from the failure information of failed bit locations within the memory array or adding failed bit locations of the failed address, however Shephard does disclose identifying failed addresses within the memory array (See Col. 3, lines 18-20). Shephard also does not explicitly teach the BIST being connected to a computer tester via a communications link, however Shephard does teach the system being programmable and instructions being scanned into the system (See Col. 1, lines 50-51 and Col. 2, lines 48-49), this is interpreted as the system being connected to an outside tester via a link.

Swoboda teaches methods that provide improved testability of systems (See Col. 2, line 60 to Col. 3, line 15). Swoboda teaches the system including a host computer attached to the system under test for emulation, which is interpreted as a computer tester communicatively linked to chip for testing (See Fig. 2, and Col. 7, lines 28-43).

Bhavsar teaches testing a memory with a BIST and generating bit-map of the failed memory, it is interpreted that the bit-map contains the failed bits of the failed memory location (See Col. 4, lines 30-32).

It would be obvious to one of ordinary skill in the art at the time of the invention to combine the bit-map generating of Bhavsar and the computer tester and communications link of Swoboda with the testing method of Shephard. This would have been obvious to do because it allows for a repair solution to be determined (See Bhavsar Col. 1, lines 48-49) and because it allows the programs to be scanned into the target chip (See Swoboda, Col. 8, lines 23-54).

28. Referring to claim 15, Shephard and Swoboda teach all the limitations (See rejection of claim 14) except for the generating a bit-map from the failure information of failed bit locations within the memory array, however Shephard does disclose identifying failed addresses within the memory array (See Col. 3, lines 18-20). Bhavsar teaches testing a memory with a BIST and generating bit-map of the failed memory (See Col. 4, lines 30-32). It would be obvious to one of ordinary skill in the art at the time of the invention to combine the bit-map generating of Bhavsar with the medium of Shephard and Swoboda. This would have been obvious to one of ordinary skill in the art at the time of the invention to do because it allows for a repair solution to be determined (See Bhavsar, Col. 1, lines 48-49).

29. Referring to claim 18, Shephard and Swoboda disclose all the limitations (See rejection of claim 17) except for adding failed bit locations of the failed address, however Shephard does disclose identifying failed addresses within the memory array (See Col. 3, lines 18-20). Bhavsar teaches testing a memory with a BIST and generating bit-map of the failed memory, it is interpreted that the bit-map contains the failed bits of the failed memory location (See Col. 4, lines 30-32). It would be obvious to one of ordinary skill in the art at the time of the invention to combine the bit-map generating of Bhavsar with the medium of Shephard and Swoboda. This would have been obvious to one of ordinary skill in the art at the time of the invention to do because it allows for a repair solution to be determined (See Bhavsar, Col. 1, lines 48-49).

30. Referring to claim 19, Shephard and Swoboda disclose all the limitations (See rejection of claim 13) except for repairing the chip using redundancy allocation techniques based on the set of failure information. Bhavsar teaches using spare rows and/or columns to replace failed ones (See Col. 2, lines 22-29). Bhavsar also teaches the repair solution being based on extracted failure information from the test (See Col. 4, lines 64-65). It would be obvious to one of ordinary skill in the art at the time of the invention to combine the repair scheme with redundancy of Bhavsar with the medium of Shephard and Swoboda. This would have been obvious to one of ordinary skill in the art at the time of the invention to do this because the scheme of Bhavsar provides a higher yield of chips during manufacture (See Col. 2, lines 2-5).

31. Referring to claim 22, Shephard and Swoboda disclose all the limitations (See rejection of claim 21) except for repairing the chip using redundancy allocation techniques based on the set of failure information. Bhavsar teaches using spare rows and/or columns to replace failed ones (See Col. 2, lines 22-29). Bhavsar also teaches the repair solution being based on extracted failure information from the test (See Col. 4, lines 64-65). It would be obvious to one of ordinary skill in the art at the time of the invention to combine the repair scheme with redundancy of Bhavsar with the system of Shephard and Swoboda. This would have been obvious to one of ordinary skill in the art at the time of the invention to do this because the scheme of Bhavsar provides a higher yield of chips during manufacture (See Col. 2, lines 2-5).

32. Referring to claim 35, Shephard and Swoboda teach all the limitations (See rejection of claim 21) except for the generating a bit-map from the failure information of failed bit locations within the memory array, however Shephard does disclose identifying failed addresses within the memory array (See Col. 3, lines 18-20). Bhavsar teaches testing a memory with a BIST and generating bit-map of the failed memory (See Col. 4, lines 30-32). It would be obvious to one of ordinary skill in the art at the time of the invention to combine the bit-map generating of Bhavsar with the testing method of Shephard and Swoboda. This would have been obvious to one of ordinary skill in the art at the time of the invention to do because it allows for a repair solution to be determined (See Bhavsar, Col. 1, lines 48-49).

33. Referring to claim 36, Shephard, Swoboda, and Bhavsar teach all the limitations (See rejection of claim 35) including using a fault bit map for cutting fuses to repair the RAM, this is interpreted as a redundancy allocation algorithm that generates a fuse map for repairing the failed addresses (See Bhavsar, Col. 4, lines 30-38).

34. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shephard and Swoboda in view of Bosse, U.S. Patent 4,586,178.

35. Referring to claim 9, Shephard and Swoboda teach all the limitations (See rejection of claim 1) except for identifying a number of circuit redundancies within the chip and halting the testing if the failure information exceeds the number of

redundancies. Bosse discloses aborting a test if assigning a redundant row or column to repair a faulty original one is not possible because the supply of redundant rows or columns has been exhausted (See Col. 8, lines 44-52). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the redundant memory and aborting a test of Bosse with the chip testing method of Shephard and Swoboda. This would have been obvious to one of ordinary skill in the art at the time of the invention to do because it alerts the user to the fact that it is not possible to repair the memory (See Bosse, Col. 9, lines 3-6).

Allowable Subject Matter

36. Claims 25, 30, 33, and 37 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

37. Applicant's arguments, see pages 8-11 of amendment, filed 07 June 2004, with respect to the rejection(s)of claim(s) 1-3, 5-6, 13-14, 16-17, and 20-21 under 35 U.S.C. 102 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Swoboda, See above rejection.

38. Applicant's arguments, see pages 8-14 of amendment, filed 07 June 2004, with respect to the rejection(s)of claim(s) 4, 7-8, 12, 15, 18-19, and 22 under 35 U.S.C. 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Swoboda, See above rejection.

39. Applicant's arguments, see page 14 of amendment, filed 07 June 2004, with respect to the rejection(s)of claim(s) 9 under U.S.C. 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Swoboda, See above rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Manoskey whose telephone number is (703) 308-5466. After Approximately October 15, 2004, the examiner can be reached at the new Alexandria telephone number, (571) 272-3648. The examiner can normally be reached on Mon.-Fri. (8am to 4:30pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JDM
August 26, 2004

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